Amendments to the Claims

1. *(Currently Amended)* A serial communication system comprising: a serial communication bus ~~(24)~~ having at least a first set of traces ~~(28)~~ and a second set of traces ~~(26);~~ a first serial communication device ~~(20),~~ fabricated as a first integrated circuit and connected to a first end of said serial communication bus ~~(24),~~ for transmitting and receiving serial data streams via said first set of traces ~~(28)~~ and said second set of traces ~~(26),~~ respectively; and a second serial communication device ~~(22),~~ fabricated as a second integrated circuit and connected to a second end of said serial communication bus ~~(24)~~, for receiving and transmitting serial data streams via said first set of traces ~~(28)~~ and said second set of traces ~~(26),~~ respectively, wherein said first serial communication device ~~(20)~~ has been pin configured to operate as a root device and said second serial communication device ~~(22)~~ has been pin configured to operate as an endpoint device.

2. *(Original)* The serial communication system of claim 5, wherein said first and second integrated circuits have identical architectures.

3. *(Currently Amended)* The serial communication system of claim 1, wherein both said first and second serial communication devices ~~(20,22)~~ include at least one state machine having state transitions which occur as a function of said pin configured device type.

4. *(Currently Amended)* The serial communication system of claim 3, wherein said at least one state machine includes a SEND_SLOT_PWR state which can be reached by said first serial communication device ~~(20)~~ but not by said second serial communication device ~~(22).~~

5. *(Currently Amended)* The serial communication system of claim 1, wherein said first serial communication device ~~(20)~~ is enabled to transmit a first set of messages and said second serial communication device ~~(22)~~ is enabled to transmit a second set of messages.

6. *(Original)* The serial communication system of claim 5, wherein said first set of messages includes at least one configuration message and said second set of messages includes at least one interrupt message.

7. *(Currently Amended)* The serial communication system of claim 5, wherein said second set of messages includes a PME message which requests said first serial

communication device ~~(20)~~ to perform a power management state change and wherein said first set of messages includes a PME_Turn_Off message, which message instructs said second serial communication device ~~(22)~~ to stop sending said PME messages.

8. *(Currently Amended)* A serial communication device comprising: means for selectively operating said serial communication device ~~(20 or 22)~~ in either a root device mode or an endpoint device mode; means for, when said serial communication device is operating in said root device mode, transmitting a first set of messages; and means for, when said serial communication device is operating in said endpoint device mode, transmitting a second set of messages different than said first set of messages.

9. *(Original)* The serial communication device of claim 8, wherein said means for selectively operating further comprises: a set of bits in a PCI Express capabilities register which are set to a first value when said serial communication device is operating in said root device mode and which are set to a second value when said serial communication device is operating in said endpoint device mode.

10. *(Original)* The serial communication device of claim 9, wherein said set of bits in said PCI Express capabilities register is set via a pin at power on of said serial communication device.

11. *(Original)* The serial communication device of claim 8, wherein said first set of messages includes a configuration request message and said second set of messages includes an interrupt message.

12. *(Original)* The serial communication device of claim 8, wherein both said first and second serial communication devices include at least one state machine having state transitions which occur as a function of device mode.

13. *(Original)* The serial communication device of claim 12, wherein said at least one state machine includes a SEND_SLOT_PWR state which can be reached by said serial communication device only when said serial communication device is operating in said root mode

14. *(Currently Amended)* A method for communicating between serial devices comprising the steps of: configuring a first serial device ~~(20)~~ to -operate in a root operating

mode and a second serial device ~~(22)~~ to operate in an endpoint operating mode; transmitting a first set of messages from said first serial device ~~(20)~~ to said second serial device ~~(22)~~; and transmitting a second set of messages from said second serial device ~~(22)~~ to said first serial device ~~(20)~~.

15. *(Currently Amended)* The method of claim 14, wherein said first serial device ~~(20)~~ and said second serial device ~~(22)~~ have identical architectures.

16. *(Original)* The method of claim 14 wherein said step of configuring further comprises: setting a set of bits in a PCI Express capabilities register of said first serial device to a first value for said first serial device operating in said root mode and setting said set of bits in another PCI Express capabilities register of said second serial device to a second value for said second serial device operating in said endpoint mode.

17. *(Original)* The method of claim 16, wherein said set of bits in said PCI Express capabilities register is set via a pin at power on of said first and second serial devices.

18. *(Original)* The method of claim 14, wherein said first set of messages includes a configuration request message and said second set of messages includes an interrupt message.

19. *(Original)* The method of claim 14, wherein both said first and second serial devices include at least one state machine having state transitions which occur as a function of device mode.

20. *(Original)* The method of claim 19, wherein said at least one state machine includes a SEND_SLOT_PWR state which can be reached by said serial communication device only when said serial communication device is operating in said root mode.